Thereafter, as shown in Fig. 5B, after the source/drain regions and the control gate have been formed, isotropic etching is used to remove part of the tunnel oxide film 2 under a sidewall of the floating gate 3 (e.g., pg. 17, lines 6-18; and pg. 21, lines 11-16). Due to this removal of the damaged part of the tunnel oxide film 2, there is less of a path for electrons to leak from the floating gate 3 to the substrate 1 during operation of the finished product (e.g., pg. 21, lines 17-19). After part of the tunnel oxide film 2 has been removed as shown in Fig. 5B, a second insulating film 10 is formed. Then, a thermal oxidation process is performed as shown in Fig. 5D in order to oxidize sidewalls of the gate 3 thereby forming oxide layer 11. Due to the steps performed in Figs. 5B-5D, substantially uniform oxidation occurs at the interface between the floating gate 3 and the surrounding insulating films; therefore, substantially equal FN (Fowler-Nordheim) currents flow through the tunnel oxide film 2 during write operations (e.g., pg. 21, line 19 to pg. 22, line 2). As a result, variation in threshold voltage compared to conventional memories can be reduced, write time can be shortened, and/or cells affected by gate disturbance can be reduced (e.g., pg. 22, lines 2-11).

Specification Objections & Allowable Claim 2

With respect to paragraph 1 of the Office Action, the specification has been amended as suggested by the Examiner.

Claim 1 stands objected to in paragraph 2 of the Office Action. It is respectfully submitted that such objections are addressed and overcome by the changes to claim 1 herein.

Applicant notes with appreciation the Examiner's indication that claim 2 contains allowable subject matter. Claim 2 has essentially been rewritten in independent form, and is thus in condition for allowance.

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Chen. This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "forming the control gate in stripes composed of the second conductive layer, the first insulating film in stripes and the floating gate in a rectangular solid composed of the first conductive layer by etching with a mask in stripes extending a direction perpendicular to the first conductive layer; ***after*** said forming of the source/drain region, removing a portion of the tunnel oxide film immediately ***under*** part of the floating gate by isotropical etching; and depositing a second insulating film on the control gate, sidewalls of the first insulating film, the floating gate and the tunnel oxide film to be covered with the second insulating film." For example, see Figs. 4-5 which illustrate tunnel oxide film 2, floating gate 3, control gate 8 and source/drain 9. *After* formation of the S/D, Figs. 5A-5B illustrate that a portion of the tunnel oxide film 2 is removed immediately under part of the floating gate 3 by isotropical etching.

Due to this removal of a potentially damaged part of the tunnel oxide film 2, there is less of a path for electrons to leak from the floating gate 3 to the substrate 1 during operation of the finished product (e.g., pg. 21, lines 17-19). After part of the tunnel oxide film 2 has been removed as shown in Fig. 5B, a second insulating film 10 may be formed.

Then, a thermal oxidation process may be performed as shown in Fig. 5D in order to oxidize sidewalls of the gate 3 thereby forming oxide layer 11. Accordingly, substantially uniform oxidation occurs at the interface between the floating gate 3 and the surrounding insulating films; therefore, substantially equal FN (Fowler-Nordheim) currents flow through the tunnel oxide film 2 during write operations (e.g., pg. 21, line 19 to pg. 22, line 2). As a result, variation in threshold voltage compared to conventional memories can be reduced, write time can be shortened, and/or cells affected by gate disturbance can be reduced (e.g., pg. 22, lines 2-11).

Chen discloses a method of making an EEPROM including tunnel oxide 120, floating gate 122, insulator 124 and control gate 126 (e.g., see Fig. 4D). Chen illustrates in Fig. 4A that a resist 710 is used so that etching removes part of the tunnel oxide 120 along with field oxide 300 in areas over the substrate where source regions are subsequently to be formed (e.g., col. 6, lines 36-42; and col. 7, lines 43-58). However, Chen significantly differs from the invention of claim 1 in that Chen's etching of tunnel oxide 120 is performed in Fig. 4A using resist 710 solely for the purpose of removing the tunnel oxide from areas where the source region is *subsequently* to be formed. In other words, Chen's removal of part of the tunnel oxide 120 must be done *before* the source/drain region is formed (see Figs. 4A and 4B of Chen) – not "after" as required by claim 1. Thus, it can be seen that Chen teaches directly away from the invention of claim 1. Moreover, one of ordinary skill in the art would never have modified Chen to meet claim 1, because to do so would destroy the purpose sought by Chen's process.

Furthermore, Chen also fails to disclose or suggest removing a portion of the tunnel oxide film immediately *under* part of the floating gate by isotropical etching as required by claim 1.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph beginning at page 1, line 13:

[0002] Conventionally, a nonvolatile semiconductor memory of this kind is manufactured according to a process order shown in Figs. 10A to [10B]10C and 11A to 11C. Figs. 10A to 10C are cross sections in an X-X direction in Fig. 1A. Figs. 11A to 11C are cross sections in a Y-Y direction in Fig. 1A. Here, Fig. 1A is a plan view of a nonvolatile semiconductor memory according to an embodiment of the present invention, but Fig. 1A is also used to explain a conventional technique.

The paragraph beginning at page 2, line 15:

[0005] Subsequently, photolithography is performed to form a photoresist (not shown) in stripes extending in the Y-Y direction. Arsenic (As) ion implantation is performed by using this photoresist and the first conductive layer 3 patterned in stripes as masks under conditions of an acceleration energy 15 keV and a dose of 4.5×10^{15} ions/cm^2 so as to form an n-type high-concentration impurity diffusion layer 5 in the low-concentration impurity diffusion layer 4. These impurity diffusion layers 4, 5 are used as [the]a source/drain region i.e. a bit line.

The paragraph beginning at page 18, line 7:

[0055] Subsequently, as shown in Fig. 5D, thermal oxidation is performed in an oxygen atmosphere at e.g. 850°C for 20 minutes so as to oxidize the sidewalls of the floating gate 3 and the control gate 8 composed of polysilicon via the second insulating film 10. Consequently, a silicon oxide film 11 composed of polysilicon having a thickness of 20 to 30 nm is formed on sidewalls of the floating gate 3 and the control gate 8. In this case, as shown in Fig. [6A]6 which is an enlarged view of a portion P2 enclosed with a broken line in Fig. 5C, oxidation of the grain boundary 13 between polysilicon grains 12 constituting the floating gate 3 is suppressed and uniform oxidation occurs at the interface between the floating gate 3 and its surrounding insulating films [10, 2]10 and 11.

IN THE CLAIMS

1. (Amended) A method for manufacturing a nonvolatile semiconductor memory [wherein]including memory cells formed in a matrix on a semiconductor substrate, wherein each [having]memory cell comprises a tunnel oxide film, a floating gate, a first insulating film and a control gate stacked in this order[are formed in a matrix on a semiconductor substrate], the method comprising[the steps of]:

forming the tunnel oxide film on the semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate on the tunnel oxide film;

patterning the first conductive layer in stripes extending in one direction;

forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film on the first conductive layer;

forming a second conductive layer on the first insulating film;

forming the control gate in stripes composed of the second conductive layer, the first insulating film in stripes and the floating gate in a rectangular solid composed of the first conductive layer by etching with a mask in stripes extending a direction perpendicular to the first conductive layer;

after said forming of the source/drain region, removing a portion of the tunnel oxide film immediately [below a sidewall of]under part of the floating gate by isotropical etching; and

depositing a second insulating film on the control gate, sidewalls of the first insulating film, the floating gate and the tunnel oxide film to be covered with the second insulating film.

2. (Amended) A method for manufacturing a nonvolatile semiconductor memory wherein memory cells formed in a matrix on a semiconductor substrate wherein each memory cell comprises a tunnel oxide film, a floating gate, a first insulating film and a control gate stacked in this order, the method comprising:

forming the tunnel oxide film on the semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate on the tunnel oxide film;

patterning the first conductive layer in stripes extending in one direction;

forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film on the first conductive layer;

forming a second conductive layer on the first insulating film;

forming the control gate in stripes of the second conductive layer, the first insulating film in stripes and the floating gate in a rectangular solid of the first conductive layer by etching with a mask in stripes extending a direction perpendicular to the first conductive layer;

removing a portion of the tunnel oxide film immediately below a sidewall of the floating gate by isotropical etching;

depositing a second insulating film on the control gate, sidewalls of the first insulating film, the floating gate and the tunnel oxide film to be covered with the second insulating film; and

[The method for manufacturing a nonvolatile semiconductor memory according to Claim 1,]wherein after the second insulating film is deposited, thermal oxidation is performed to oxidize the sidewall of the floating gate via the second insulating film.

Please add the following new claims:

5. (New) A method for manufacturing a nonvolatile semiconductor memory comprising at least one memory cell including a tunnel oxide film, a floating gate, a first insulating film and a control gate, the method comprising:

forming the tunnel oxide film so as to be supported by at least a semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate over the tunnel oxide film;

patterning the first conductive layer;

forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film over at least the first conductive layer;

forming a second conductive layer over at least the first insulating film, and patterning the second conductive layer to form at least one control gate;

after said forming of the source/drain region and after the floating gate has been formed via the first conductive layer, removing a portion of the tunnel oxide film immediately under part of the floating gate by etching; and

depositing a second insulating film over at least the control gate, at least one sidewall of the first insulating film, at least one sidewall of the floating gate and at least one sidewall of the tunnel oxide film.

6. (New) The method of claim 5, wherein after the second insulating film is deposited, thermal oxidation is performed to oxidize the sidewall of the floating gate via the second insulating film.

7. (New) The method of claim 5, wherein said etching used to remove the portion of the tunnel oxide film comprises isotropic etching by wet etching using at least a fluorinated acid.

8. (New) The method of claim 5, wherein the second insulating film comprises silicon oxide, and is formed via chemical vapor deposition.